

What is claimed is:

1       1. A bi-directional communication link having plural  
2       channels, each of said channels comprising:

3               a master connected at a near of the channel and a  
4       slave connected at an opposite end of the channel;

5               said master comprising:

6               (a) a transmitter coupled to the channel and  
7       having a master Tx clock signal;

8               (b) a receiver coupled to the channel and  
9       comprising:

10               (i) an analog-to-digital converter that  
11       periodically samples at a sampling time  $T_s$ ;

12               (ii) a clock recovery circuit that  
13       generates a master Rx clock from a clock signal embedded in a  
14       signal received from the channel;

15               (iii) a metric processor connected to an  
16       output of said analog-to-digital converter that produces a  
17       metric signal indicative of resolution of the received  
18       signal;

19               said slave comprising:

20               (a) a receiver coupled to the channel and  
21       comprising a clock recovery circuit for generating a Slave Rx  
22       clock from the signal received from the master;

23               (b) a transmitter coupled to the channel and  
24       having a Slave Tx clock signal, whereby said master Rx clock  
25       signal is frequency locked to said Slave Tx clock signal;

26               (c) a controllable delay element for  
27       generating said Slave Tx clock signal from said Slave Rx  
28       clock signal;

29               said communication link further comprising a  
30       decision processor responsive to said metric processor for  
31       changing a delay value of said controllable delay element so  
32       as to maximize the metric signal.

1       2. The apparatus of claim 1 wherein said resolution is a  
2       resolution between leading and trailing edges of the received  
3       signal.

1       3. The apparatus of claim 1 wherein said resolution is a  
2       resolution between allowed amplitude levels of the received  
3       signal.

1       4. The apparatus of claim 1 further comprising a second  
2       controllable delay between said Master Rx clock signal and  
3       said analog-to-digital converter and responsive to said  
4       decision processor, whereby said decision processor delays  
5       the Slave Tx clock signal and the sample time Ts  
independently to maximize the metric signal.

1       5. A bi-directional communication link having plural  
2       channels with respective masters and slaves at respective  
3       ends of respective channels, each master issuing a Master Tx  
4       clock, each slave constructing a Slave Rx clock  
5       frequency-locked to the Master Tx clock, and a Slave Tx clock  
6       frequency-locked to the Slave Rx clock, said bi-directional  
7       communication link comprising:  
8              a metric processor for each master that produces a  
9       metric signal indicative of resolution of a signal received  
10      by the master from the corresponding slave; and

11              a decision processor responsive to said metric  
12       processor for changing the phase of the Slave Tx clock  
13       relative to the Slave Rx clock so as to maximize the metric  
14       signal.

1       6. The apparatus of claim 5 wherein said resolution is a  
2       resolution between leading and trailing edges of the received  
3       signal.

1       7. The apparatus of claim 5 wherein said resolution is a  
2 resolution between allowed amplitude levels of the received  
3 signal.

1       8. A bi-directional communication link having plural  
2 channels with respective masters and slaves at respective  
3 ends of respective channels, each master issuing a Master Tx  
4 clock, each slave constructing a Slave Rx clock  
5 frequency-locked to the Master Tx clock, and a Slave Tx clock  
6 frequency-locked to the Slave Rx clock, wherein the master  
7 samples a signal it receives from the slave at a sample time  
8 Ts frequency locked to the Master Rx clock, said  
9 bi-directional communication link comprising:

10            a metric processor for each master that produces a  
11 metric signal indicative of resolution of a signal received  
12 by the master from the corresponding slave; and

13            a decision processor responsive to said metric  
14 processor for shifting said sample time Ts relative to the  
15 Master Tx clock so as to maximize the metric signal.

16       9. The apparatus of claim 8 wherein said resolution is a  
17 resolution between leading and trailing edges of the received  
18 signal.

19       10. The apparatus of claim 8 wherein said resolution is a  
20 resolution between allowed amplitude levels of the received  
21 signal.

22       11. A bi-directional communication link having plural  
23 channels with respective masters and slaves at respective  
24 ends of respective channels, each master issuing a Master Tx  
25 clock, each slave constructing a Slave Rx clock  
frequency-locked to the Master Tx clock, and a Slave Tx clock  
frequency-locked to the Slave Rx clock, wherein each master  
receives a periodic noise burst comprising cross-talk from

8 masters of adjacent channels and echoes of itself, said noise  
9 capable of reducing the resolution of a signal received by  
10 the master from the slave over the corresponding  
11 communication, said bi-directional communication link  
12 comprising:

13 a metric processor for each master that produces a  
14 metric signal indicative of the resolution of the signal  
15 received by the master from the corresponding slave; and

16 a decision processor responsive to said metric  
17 processor for changing the phase of the Slave Tx clock  
18 relative to the Slave Rx clock so as to reduce the effects of  
19 the noise burst on the received signal and thereby increase  
20 the metric signal.

12. The apparatus of claim 11 wherein said resolution is a  
resolution between leading and trailing edges of the received  
signal.

13. The apparatus of claim 11 wherein said resolution is a  
resolution between allowed amplitude levels of the received  
signal.

14. A bi-directional communication link having plural  
channels with respective masters and slaves at respective  
3 ends of respective channels, each master issuing a Master Tx  
4 clock, each slave constructing a Slave Rx clock  
5 frequency-locked to the Master Tx clock, and a Slave Tx clock  
6 frequency-locked to the Slave Rx clock, wherein the master  
7 samples a signal it receives from the slave at a sample time  
8 Ts frequency locked to the Master Rx clock, and wherein each  
9 master receives a periodic noise burst comprising cross-talk  
10 from masters of adjacent channels and echoes of itself, said  
11 noise capable of reducing the resolution of a signal received  
12 by the master from the slave over the corresponding

13 communication, said bi-directional communication link  
14 comprising:

15 a metric processor for each master that produces a  
16 metric signal indicative of the resolution of the signal  
17 received by the master from the corresponding slave; and

18 a decision processor responsive to said metric  
19 processor for shifting said sample time Ts relative to the  
20 Master Tx clock so as to reduce the effects of the noise  
21 burst on the received signal and thereby increase the metric  
22 signal.

1 15. The apparatus of claim 14 wherein said resolution is a  
2 resolution between leading and trailing edges of the received  
3 signal.

4 16. The apparatus of claim 14 wherein said resolution is a  
5 resolution between allowed amplitude levels of the received  
6 signal.

7 17. The apparatus of claim 14 further comprising a  
8 controllable delay between said Slave Rx clock and said Slave  
9 Tx clock, said decision processor governing said controllable  
10 delay so as the shift said sample time Ts.

11 18. The apparatus of claim 15 wherein said metric processor  
12 comprises a processor for computing an opening in an eye  
13 diagram of the signal received by the master.

14 19. The apparatus of claim 16 wherein said metric processor  
15 comprises a processor for computing the proportion of samples  
16 of the signal received by the master falling within allowed  
17 amplitude levels relative to those that fall outside of  
18 allowed amplitude levels.

1       20. In a bi-directional communication link having plural  
2       channels with respective masters and slaves at respective  
3       ends of respective channels, each master issuing a Master Tx  
4       clock, each slave constructing a Slave Rx clock  
5       frequency-locked to the Master Tx clock, and a Slave Tx clock  
6       frequency-locked to the Slave Rx clock, wherein the master  
7       samples a signal it receives from the slave at a sample time  
8        $T_s$  frequency locked to the Master Rx clock, and wherein each  
9       master receives a periodic noise burst comprising cross-talk  
10      from masters of adjacent channels and echoes of itself, said  
11      noise capable of reducing the resolution of a signal received  
12      by the master from the slave over the corresponding  
13      communication, a method of reducing the effects of the  
14      cross-talk and echo noise burst on the signal received by  
15      each master, comprising:  
16                  for each master, producing a metric signal  
17                  indicative of the resolution of the signal received by the  
18                  master from the corresponding slave; and  
19                  in response to said metric signal, shifting said  
20                  sample time  $T_s$  relative to the Master Tx clock so as to  
21                  reduce the effects of the noise burst on the received signal  
22                  and thereby increase the metric signal.

23       21. The method of claim 20 wherein said resolution is a  
24       resolution between leading and trailing edges of the received  
25       signal.

26       22. The method of claim 20 wherein said resolution is a  
27       resolution between allowed amplitude levels of the received  
28       signal.

29       23. The method of claim 20 wherein the shifting of said sample  
30       time  $T_s$  is carried out by changing a delay between said Slave  
31       Rx clock and said Slave Tx clock.

1       24. The method of claim 21 wherein the producing of the  
2 metric signal comprises computing an opening size in an eye  
3 diagram of the signal received by the master.

1       25. The method of claim 22 wherein the producing of the  
2 metric signal comprises computing the proportion of samples  
3 of the signal received by the master falling within allowed  
4 amplitude levels relative to those that fall outside of  
5 allowed amplitude levels.

1       26. In a bi-directional communication link having plural  
2 channels with respective masters and slaves at respective  
3 ends of respective channels, each master issuing a Master Tx  
4 clock, each slave constructing a Slave Rx clock  
5 frequency-locked to the Master Tx clock, and a Slave Tx  
clock frequency-locked to the Slave Rx clock, wherein the  
master samples a signal it receives from the slave at a  
sample time  $T_s$  frequency locked to the Master Rx clock, and  
wherein each master receives a periodic noise burst  
comprising cross-talk from masters of adjacent channels and  
echoes of itself, said noise capable of reducing the  
resolution of a signal received by the master from the slave  
over the corresponding communication, a method of reducing  
the effects of the cross-talk and echo noise burst on the  
signal received by each master, comprising:  
15

16                 for each master, producing a metric signal  
17 indicative of the resolution of the signal received by the  
18 master from the corresponding slave;

19                 for each slave, producing a metric signal  
20 indicative of the resolution of the signal received by the  
21 slave from the corresponding master; and

22                 in response to the metric signal corresponding to  
23 the master and to the metric signal corresponding to the  
24 slave, shifting said sample time  $T_s$  relative to the  
25 Master Tx clock so as to reduce the effects of the noise

26      burst on the received signal at both the master and the  
27      slave and thereby increase the metric signals corresponding  
28      to the master and the slave.

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